# Investigation of the behaviors of various electroplated copper films during CMP

H. P. Feng*, M. Y. Cheng**, Y. Y. Wang*** and C. C. Wan****

* Department of Chemical Engineering, National Tsing Hua University,
Hsinchu,Taiwan, hpfeng@tsmc.com
** Department of Materials Science and Engineering, National Chiao Tung University,
Hsinchu, Taiwan, mychenga@tsmc.com
*** Department of Chemical Engineering, National Tsing Hua University,
Hsinchu,Taiwan, ccwan@nthu.edu.tw
**** Department of Chemical Engineering, National Tsing Hua University,
Hsinchu,Taiwan, yywang@nthu.edu.tw

## ABSTRACT

The behaviors of various electroplated copper films during CMP are important for removal mechanism and defect generation. This article was to study the characteristics of various copper films during CMP, including impurity effect and current density effect. Potentiodynamic polarization method was used to understand the removal behaviors. XRD and SIMS were applied to investigate the film texture and impurity content. Defect performance was decided in optical scan method and SEM reviewing. The research showed that (111)/(200) texture ratio determined removal rate and voids located in grain boundaries. Removal rate and void defects decreased with increasing (111)/(200) ratio. High (111)/(200) ratio has strong chemical resistance during polishing because (111) is the closed packed plane in the fcc structure. For impurity study, carbon and sulfur are impure atoms to weaken Cu grain boundaries to generate more void defects, but are insufficient to determine the removal rate. Furthermore, a novel phenomenon was observed that interconnect surface generate copper extrusion with time after polishing. AES proved that the sulfur content of grain boundaries induce this reaction. Based on above studies, we attempt to describe the relation between copper film properties and polishing performance.

***Keywords***: copper plating, texture, impurity, removal rate, current density, defect

## 1 INTRODUCTION

Copper has replaced aluminum as the interconnect metal in integrated circuits due to its higher electrical conductivity and superior electromigration resistance. Electroplating has been adopted by industry as the primary deposition method for Cu metallization technology. Microstructure control of electroplated Cu with different variables has been a focus of interest. Polishing performance, including defect generation and removal rate, has high correlation to copper film microstructure and slurry characteristic. Haebum Lee and S. Simon Wong [1] reported that a strong correlation between stress and texture development was found for all electroplated Cu films with different conditions during self-annealing and post thermal annealing process. For fcc metal films, the orientation with the lowest surface energy is (111) while that with the lowest elastic strain energy is (100) [2,3]. As the film stress exceeds a critical value, the (111) texture degrades and (200) texture enhances to minimize the total energy [4,5]. Film stress is also affected by the Cu/TaN barrier interface bond strength [6]. It indicated that the strong interface bonding to lead the large stress and thus degrade (111) texture [7,8]. Furthermore, copper surface chemistry plays an important role in the CMP process. A. Jindal and S. V. Babu [9] reported that the CMP removal mechanism of copper film in slurries is to form the porous surface layer leading to higher removal rate and to reduce friction softening the surface layer. During polishing, copper surface could be damaged by abrasives to cause scratches or by chemical attacking to generate corrosive voids [10]. Different texture of Cu film should have different chemical resistance during CMP. However, the performances of various copper films during CMP are not yet well understood, including film texture and impurity effect. The purpose of this article is to study the characteristics of various copper films during CMP in slurry. A removal mechanism and defect performance, based on electrochemical measurement and surface analytic technology, are proposed herein. To understand the relation between plating conditions and polishing behaviors, it could achieve free-defect in copper interconnect.

## 2 EXPERIMENT

Blanket wafers used in this study were 12-in. Si (100) wafers with 100 nm thermal oxide / 30 nm TaN / 150 nm Cu seed layer, where TaN and Cu seed layer were deposited by physical vapor deposition (PVD) without vacuum breaking. Patterned wafers with different line widths were generated by optical lithography and etch process. Cu electrochemical deposition was performed on 12-in. Si(100) wafers with seed layer using a sulfate based plating bath with a small amount of proprietary organic additives from Ethone. ECD plating-system is used to generate the Cu films was manufactured by Applied Material. CMP were carried out using the Mirra polisher with Rodel IC1010 pads in platen1,2 and politex pads in platen 3. JSR T1A and T1B-R1 alkali silica polishing slurries were used for the polishing experiments.

Static potentiodynamic polarization were performed using an EG&G Princeton Applied Research model 273 potentistat/galvanostat system. A platinum foil was used as the counter electrode and a saturated calomel electrode (SCE) was used as the reference electrode in standard three-electrode system. The removal rate of Cu film was measured by the four-point probe method using a 49 point line scan on a Prometrix resistance measurement tool. Film stress was monitored with an optical wafer curvature measuring device. X-ray diffraction was applied to determine the Cu film texture. The impurities in Cu films including carbon and sulfur atoms were detected by secondary ion mass spectrometer (SIMS) analysis. Optical scan method (KLA) was used to detect Cu film defects after CMP. Varying defect types were classified by AMAT SEMVISION reviewing tool.

## 3 RESULTS AND DISSCUSION

Figure 1 is the copper CMP removal rate versus plating films with different current density in various thicknesses. Plating films with thick thickness and high current density achieve fast removal rate. It illustrated that Cu films with different thickness and plating current have different chemical resistance. Despite film thickness or plating current, use (111)/(200) ratio as an index versus removal rate, as shown in figure 2. The removal rate is significantly related to (111)/(200) ratio. It is known that the microstructural evolution of copper film via annealing is dependent on film stress [11]. During annealing, shrinkage or densification of the film by elimination of the grain boundaries during grain growth generates stress in the film.

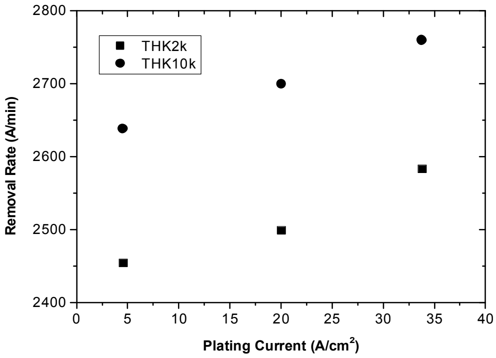

Figure 1: Removal rate versus current density and film thickness

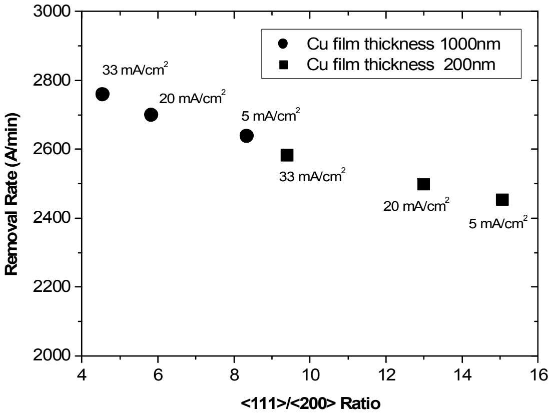

Figure 2: Value of (111)/(200) ratio versus removal rate

For fcc thin films, the (111) texture is favored by the surface and interfacial energy minimization, whereas the (200) texture is favored by the strain energy minimization [12]. It is speculate that the (111) texture has higher chemical resistance than other planes because (111) is the closed packed plane in the fcc structure [13]. To release film stress, (200) texture increase and (100) texture decrease. Therefore, thick film and high current density results in high stress to cause low (111)/(200) ratio and high removal rate. As described above, Cu film with high (111)/(200) ratio has high chemical resistance during CMP process. Figure 3 is the potentiodynamic polarization curves for copper films with various (111)/(200) ratio in slurry. The results show that corrosion current density increases with decreasing (111)/(200) ratio. The behaviors between corrosion current and removal rate are consistent with the trend of (111)/(200) ratio.

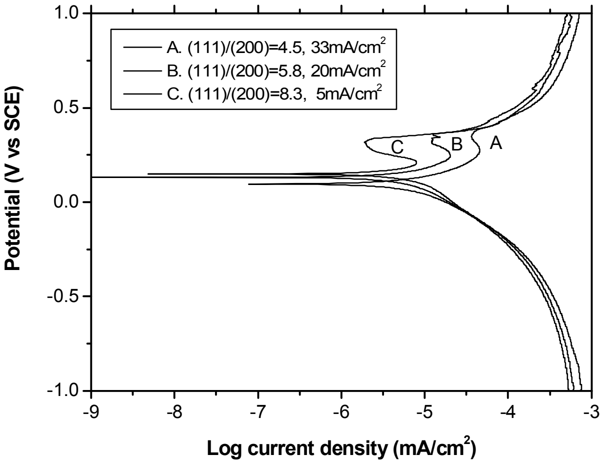

Figure 3: potentiodynamic polarization curves for copper films with various (111)/(200) ratio in slurry

During polishing, grain boundaries are easily attacked by slurry to generate voids because atoms are more loosely packed in the grain boundaries than in the crystal lattices. In brief, the copper film texture with high (111)/(200) ratio has strong chemical resistance in slurry. These findings suggested that weak chemical resistance achieve more void-defects generation. Applying different current density to generate various copper film texture in 1000nm to prove that the amount of void defects increases as the (111)/(200) ratio decreases, as shown in Figure 4. In summary, the void defects are highly associated with the texture of grain boundaries.

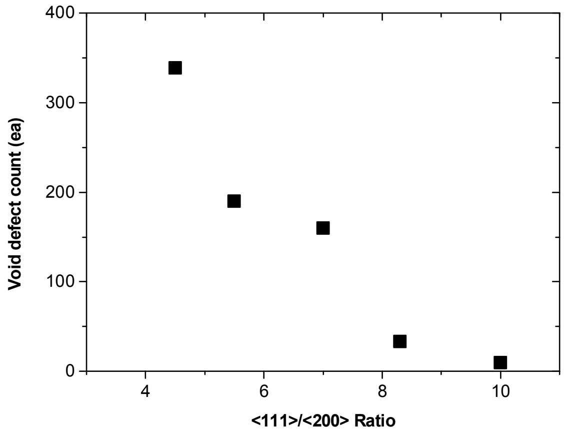

Figure 4: Amount of void defects versus (111)/(200) ratio

Moreover, understanding the role of impurities is also important to figure out the polishing performance of various Cu films. The impurity incorporation phenomenon can be explained by curvature-enhanced accelerator coverage model (CEAC) that was recently developed by West et al. and Moffat et al [14,15]. It is believed that electrolyte bath and current density are two factors for film impurities in the same annealing condition. To study impurity effect, use plating baths with four additive concentrations in identical (20 mA/cm$^2$, 1000nm) current densities and anneal condition to generate four Cu films with different impurity content in the same texture. SIMS analysis and XRD measurement showed varied carbon/sulfur content and almost the same (111)/(200) ratio for these four Cu films, as shown in Figure 5a,b. It implied that the small amount of impurities is insufficient to change the texture ratio of copper film. Figure 6 revealed that removal rate are not change with carbon/sulfur impurity, but void defects increases with raising impurity content. One reason could be that removal rate regards the performance of whole copper surface including grains and grain boundaries, but void defect is mainly related to the strength of grain boundaries. It speculated that high impurity could generate more defect during polishing because the impure atoms weaken Cu grain boundaries. In a word, impurities are insufficient to determine the removal rate due to relatively smaller area of grain boundaries. However, void defect performance during polishing could be influenced by the concentrated impurities in grain boundaries via post-plating anneal treatment.

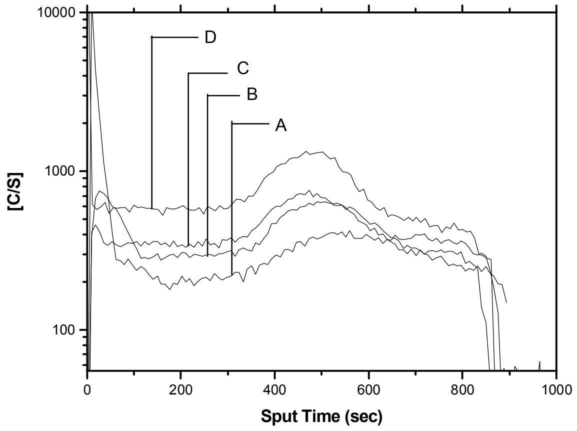

Figure 5a: SIMS carbon analysis for different Cu films

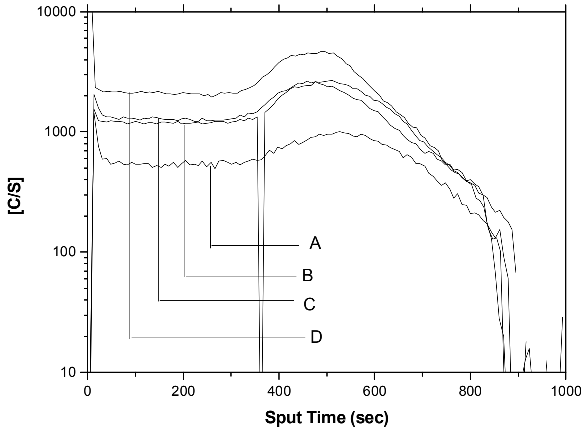

Figure 5b: SIMS sulfur analysis for different Cu films

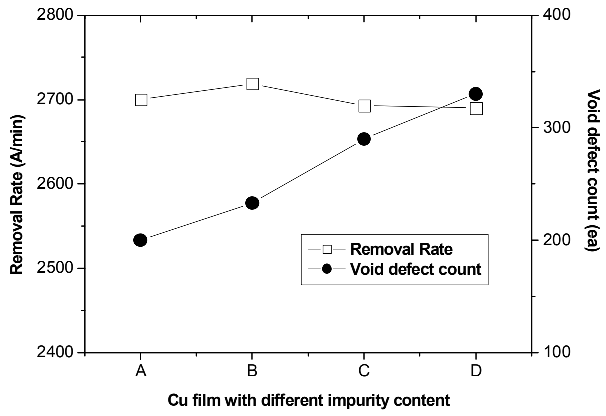

Figure 6: Removal rate and voids defect versus different impurity copper film (A<B<C<D)

Furthermore, an interesting phenomenon was observed that copper extrusion was formed in metal surface through about 12 hours after polishing, as displayed in figure 7a. Figure 7b is the Auger measurement that detected sulfur in the extrusion location as compared with normal area. In addition, the Auger mapping method provided direct evidence to prove the sulfur content of extrusion location, as shown in Figure 7c. Cu-S is not easy to remove after annealing due to its high bonding energy (276 kJ/mol) as compared with Cu-Cu (176 kJ/mol). Moreover, it was found that extrusions on narrow line are more than on wide line. According W.Zhang's report [16], the geometry effect caused high level impurities trapped in narrower line. As mention above, the phenomenon of copper extrusion is closely correlated to Sulfur impurities.

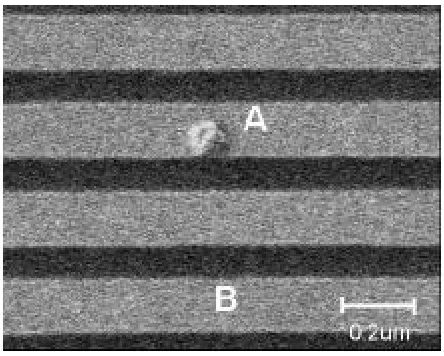

Figure 7a: SEM image of extrusion (after polishing 12hr)

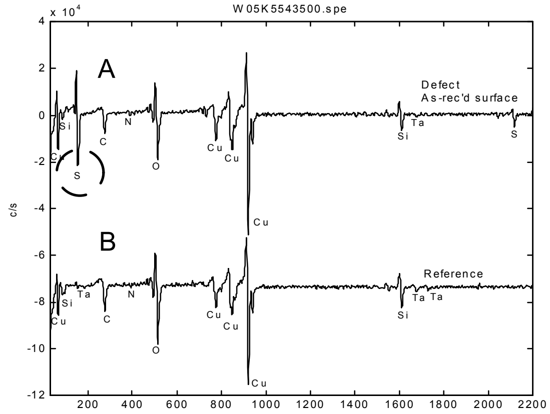

Figure 7b: AES sulfur map for extrusion area

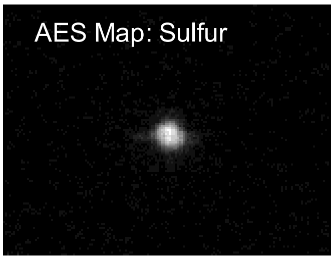

Figure7c: AES sulfur map for extrusion area

# 4 CONCLUSION

The various plating current density generated copper films with different texture and impurity content. Different copper films had different removal rate and defect performance after chemical mechanical polishing. Potentiodynamic polarization method was used to prove that corrosion current value increases with decreasing (111)/(200) ratio. The characteristics of various copper films during CMP in our studies are summarized as below:

1. Removal rate and void defects decreased with increasing (111)/(200) ratio. High (111)/(200) ratio has strong chemical resistance during polishing because (111) is the closed packed plane in the fcc structure.
2. Impurities are insufficient to determine the removal rate because of relatively smaller area of grain boundaries. But for void defects, textures and impurities are both important factors because the loosed packed or impure atoms all weaken Cu grain boundaries.
3. Sulfur impurities located in grain boundaries play the important role for the copper extrusion through a period of time after polishing.

# REFERENCES

[1] H. Lee, S.S. Wong, and S.D. Loptain, J. Appl. Phys. 93, 3796, 2003.

[2] H.L. Wei, R.K. Zheng, G.H. Wen, and X.X. Zhang, Appl. Phys. Lett. 80,2290, 2002.

[3] T. Hara, H. Toida, and Y. Shimura, J. Electrochem. Soc. 6, G98, 2003.

[4] Q.T. Jiang, and M.E. Thomas, J. Vac. Sci. Technol. B 19, 762, 2001.

[5] S.M. Rossnagel, and T.S. Kuan, J. Vac. Sci. Technol. A 20, 1911, 2002.

[6] C. Detavernier, D. Deduytsche, R.L. Van Meirhaeghe, J. De Baerdemaeker, and C. Dauwe, Appl. Phys. Lett. 82 ,1863, 2003.

[7] K.R. Hebert, J. Electrochem. Soc. 148, C726, 2001.

[8] S. Nakayama, A. Kimura, M. Shibata, S. Kuwabata, and T. Oskai, J. Electrochem. Soc. 148, B467, 2001.

[9] A. Jindal and S. V. Babu, J. Electrochem. Soc. 151, C709, 2004

[10] L. Vanasupa, Y.C. Joo, and P.R. Besser, J. Appl. Phys. 2583, 1999.

[11] M.W. Lane, C.E. Murray, F.R. McFeely, P.M. Vereecken, and R. Rosenberg, Appl. Phys. Lett. 83 2330, 2003.

[12] E.M. Zielinski, R.P. Vinci, and J.C. Bravman, J. Appl. Phys. 76, 4515, 1994.

[13] J.A. Thornton, J. Vac. Sci. Technol. 12, 830, 1975.

[14] C.West, S. Mayer, and J. Reid, Electrochem. Solid-State Lett., 4, C50, 2001

[15] T.P. Moffat, D. Wheeler, W.H. Huber, and D. Josell, Electrochem. Solid-State Lett., 4, C26, 2001

[16] W.Zang, J. Electrochem. Soc. 152, C832, 2005