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Void Defect Reduction after Chemical Mechanical Planarization of Trenches Filled by Direct/Pulse Plating

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The effect of various frequencies of pulse current (PC) on the crystal orientation of copper deposit was investigated in this article. When PC frequency was lower than 100 Hz, high (111)/(200) ratio after annealing was achieved and the amount of void defects was reduced after chemical mechanical planarization (CMP) process. In addition, the behaviors of additives depends on the pulse frequency were also studied and resulted in the different characteristics of copper deposits at various pulse frequencies. We therefore propose a modified deposition approach comprising direct current (dc) and PC which can reduce the void defects after CMP process based on the above experimental results.
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Recently, dual-damascene copper electroplating has commonly been used for on-chip metallization, in which chemical mechanical planarization (CMP) is employed to remove the protruding copper deposit and planarize the wafer surface.[1,2] The critical ability to produce void-free deposition of submicrometer-scale features usually relies on the function of specific additives in the electroplating bath.[3] The package of additives are usually composed of chloride ions (Cl^-), a suppressor, and an accelerator.[4-6] Typically polyethylene glycol (PEG) serves as a suppressor due to its strong inhibition on reaction kinetics, especially when Cl^- is present, whereas bis(3-sulfopropyl) disulfide (SPS), which works as an accelerator, accelerates the deposition.[4-10]

Unfortunately, a variety of defects are found after copper CMP process, such as micro-scratches, dishing, erosion, small particles and voids. The dishing and erosion of the interconnect materials are attributed to inconsistent removal rate and the micro-scratches may derive from the agglomeration of abrasive particles into larger particles.[11-13] As for the void defects, the occurrence has been confirmed to come from chemical attacking in slurry.[14,15] The formation and influence of void defect is shown in Fig. 1. Small void of copper surface was enlarged in the chemicals of subsequent processes, such as photolithograph and etching processes, to cause deformed copper via. The deformed copper via interrupted electron transfers between bottom and top layer on multilayer interconnect fabrication, resulting in yield loss and reliability problems. It has been reported that copper deposit with high (111) texture tends to reduce void defects after the CMP process because (111) plane belongs to closest-packed arrangement in face-centered-cubic (fcc) structure.[14,16] Many researchers have reported that the crystal orientation of copper deposits is influenced by the substrate, plating bath composition, applied current density, current waveform and annealing condition.[17-23] In particular, Oh et al.[22] reported that copper deposit plated by pulse current (PC) possesses much stronger (111) texture compared to that plated by direct current (dc) in the absence of additives.

Until now, however, the influence of PC frequency on the crystal orientation of copper deposits has not been well known. Moreover, the information regarding PC performed in the plating bath with Cl^-, PEG and SPS additives is even more lacking. In this study, we investigated the influence of pulse frequency on crystal orientation of copper deposit in plating with the above additives. In addition, the behaviors of additives at various pulse frequencies were also studied. Another objective in this study is to develop a plating scheme to obtain copper deposit with high (111) texture, which can reduce void defects after CMP process.

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Experimental

In this study, four sets of experiments were carried out. The first set was copper deposition with dc or PC on blanket wafers. The second set was to simulate the corrosion resistance of copper deposits with dc or PC at various pulse frequencies by potentiodynamic measurement in the commercial slurry. The third set was to study the electrode kinetics by cyclic voltammetry (CV) and potential response with PC at various pulse frequencies. The fourth set was to perform the proposed plating scheme on pattern wafers and then process polishing.

Deposition experiments were performed on blanket wafers, prepared by depositing a 30 nm sputtered TaN diffusion barrier layer and a 150 nm sputtered copper conduction layer on p-type silicon substrate with (100) orientation. A fragment of blanket wafer (3 $\times$ 3 cm) was first mounted on the rotating disk electrode (RDE) adaptor, basically following the design reported by Taephaisitphongse et al.[24] A copper foil was used as anode. The basic composition of the bath was 0.2 M $CuSO_4 \cdot 5H_2O$ (Fisher) and 1 M H_2SO_4 (Fisher). To modify the deposit, 50 ppm Cl^- (added as NaCl, Fisher), 350 ppm PEG (4000 Mw; Aldrich), and 2 ppm SPS (Rasching GmbH) were added into the bath. The deposition bath was operated at room temperature and the RDE adaptor was controlled at 500 rpm; then copper deposition was performed with dc or PC. The waveform of PC was controlled with a 20 mA/cm^2 cathodic peak and 0.5 duty cycle, meaning the ratio of pulse time and total time. The pulse frequencies for PC were 10, 100, 1000, and 10000 Hz.

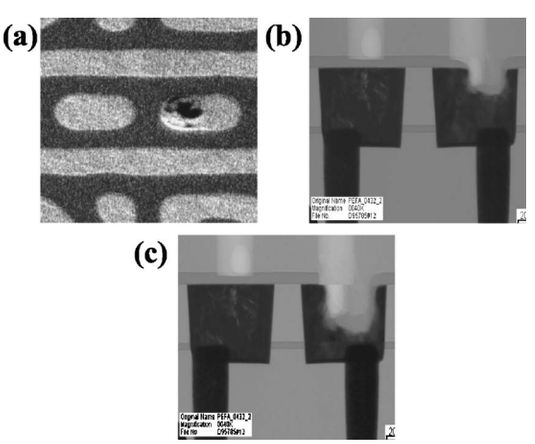

Figure 1. Images of void defect to show the influence of void defect on fabrication of multilayer interconnect. (a) Top-view of void defect. (b) Cross-sectional image of void defect. (c) Cross-sectional image of void defect after photolithograph and etching processes.

The PC was generated from a potentiostat/galvanostat (EG&G PARC model 362) controlled by a function generator (BNC Corp. model 625). The average current density of PC and dc were both 10 mA/cm^2. The copper deposits were examined by a scanning electron microscopy (SEM, Hitachi S-4000) for morphology inspection and X-ray diffraction (XRD, Philips X'pert MPD) for crystal structure. The distributions of impurities, chloride and sulfur, were detected by means of a secondary ion mass spectrometer (SIMS, CAMECA IMS-6F) analysis.

To investigate the corrosion resistance of copper deposits, the potentiodynamic polarization measurements were employed, carried out in JSR T1A alkali silica polishing slurry. In the potentiodynamic measurements, the copper deposits which had been annealed at 200°C for 1 min were scanned from 0.15 to − 0.4 V at 5 mV/s and 500 rpm. In addition, the copper deposits after annealing were placed into a special carrier to carry out polishing. Polishing experiments were achieved by utilizing the Mirra polisher with Rodel IC1010 pads in platen 1, 2 and politex pads in platen 3. The JSR commercial polishing slurries were used in the polishing experiments. The polishing results were observed by optical scan method (KLA) to detect defects on the copper deposited after CMP process. In general, types of defects formed after CMP process are scratches, particles, and void defects. Here, the void defects were only concerned in this paper.

The electrochemical kinetics measurements were performed in a three-electrode cell. A platinum RDE (0.16 cm^2) was used as working electrode along with a platinum counter electrode and a saturated calomel electrode (SCE) reference. The reference electrode was placed close to the working electrode to reduce the ohmic overpotential. Prior to the measurements of CV and potential responses during pulse plating, the working electrode was initially deposited with copper for 180 s in the predeposition bath, which contained 0.2 M $CuSO_4 \cdot 5H_2O$ and 1 M H_2SO_4. At the end of measurement, the working electrode was transferred into the stripping bath, made up of H_2O_2/H_2SO_4 = 1/3 in volume ratio, to strip off the copper. The potentials reported in this paper correspond to applied switching potential. All voltammetric experiments were performed at 1 mV/s and 500 rpm. As for measuring potential responses during pulse plating, the potential responses were stored through an analog output unit of an interface card (UEI PD2-MF-16-50/16H) in a personal computer. The maximum speed of the interface card was 50 k data s^{-1}. To ensure steady-state plating, the potential responses were stored after plating for 1 min.

To examine the performance of the proposed plating scheme, pattern wafers were used in this experiment. First, the features were filled with different times to find when the current type should be switched from dc to PC. As switched time was determined, the proposed plating scheme was employed and then the copper deposits were annealed at 200°C for 1 min. The annealed copper deposits were placed into the special carrier to carry out polishing experiment as mentioned above.

Results and Discussion

The effect of pulse frequencies on the crystal orientations of copper deposit with and without annealing is shown in Fig. 2. Apparently, (111) texture is the dominant crystal orientation in as-deposited state regardless of deposition process. Figure 2a shows that the influence of pulse frequency on crystal orientation is not significant while without annealing. It is clear the high (111)/(200) ratios, over 90, are present regardless of using any frequency. With annealing, however, the ratios of (111)/(200) at lower pulse frequencies, 10 and 100 Hz, are still high as shown in Fig. 2b. It has been reported that the microstructural evolution of copper film during annealing relies on film stress.[25,26] In particular, the elastic strain energy contributes to the change in energy during grain growth. It is well-known that copper possesses the fcc structure and (111) orientation is the closest-packed arrangement in fcc structure.[16] As for the fcc thin films, the (111) texture is favored by the surface and interfacial energy minimization, while the (200) texture is favored by the strain energy minimization.[27] The (200) texture facilitates the relaxation of strain energy, implying the (200) texture is conducive to relieve stress. Therefore, the growth of grains during annealing induces stress in the copper film in the tensile direction, and eventually changes the film into a state in which (111) texture is less favored energetically than (200) texture while film stress goes over the critical value.[27]

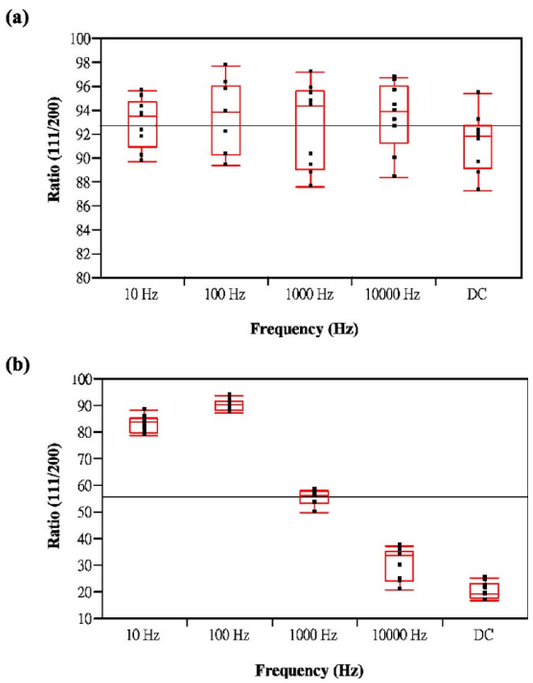

Figure 2. (Color online) Effects of PC frequency on the crystal orientation of copper deposits (a) without and (b) with annealing.

Our results indicate that dc or PC at high pulse frequency induce high stress, which leads to diminishing (111)/(200) ratio. Vainshtein et al.[28] have reported the (111) plane grows in a three-dimensional fashion while the (200) plane grows in two dimensions. Moreover, because the (111) plane is the closest-packed arrangement in fcc structure, the chemical resistance of (111) plane is higher than other planes in fcc structure.[16] The potentiodynamic measurements were applied to inspect the correlation between (111)/(200) ratio and chemical resistance. Figure 3 shows the potentiodynamic polariza-

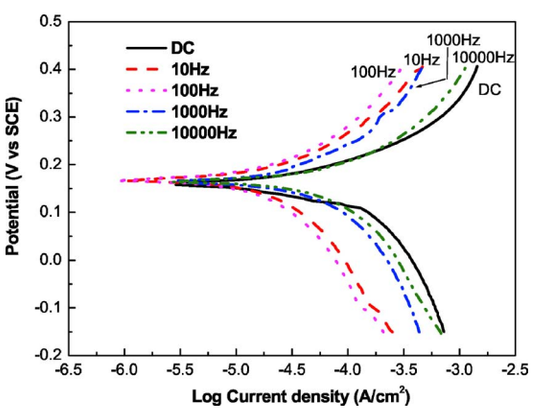

Figure 3. (Color online) Potentiodynamic polarization of copper deposits plated at various pulse frequencies after annealing immersed in commercial polishing slurry.

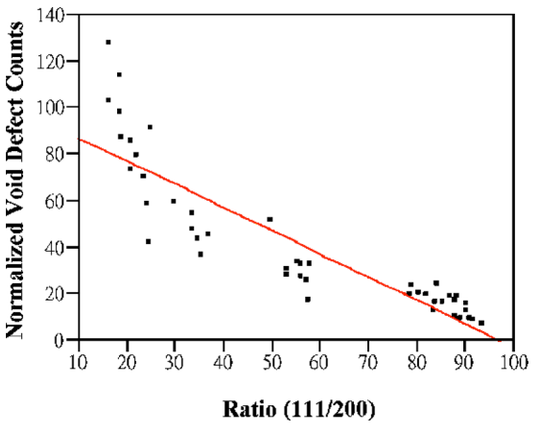

Figure 4. (Color online) Amount of void defects vs (111)/(200) ratios.

tion curves of copper films deposited with dc or PC at various pulse frequencies when immersed in the commercial CMP slurries. The results show the corrosion current densities at low frequency PC, 10 and 100 Hz, are low compared to those with dc and PC at high frequency. The behavior of corrosion current density is related to (111)/(200) ratio. In addition, the copper deposits with dc or PC at various pulse frequencies after annealing were polished by CMP. The defects were produced after the CMP process and the types of defects were detected and characterized by SEM. The correlation between the (111)/(200) ratio of copper films and the amount of void defects is summarized in Fig. 4. Apparently, the copper films with high (111)/(200) ratio have strong chemical resistance against slurry corrosion and generate few amount of void defects.

However, the use of PC to fill features is difficult. There are many parameters which should be modified.[29] To investigate the influence of pulse frequency on behaviors of additives, the potential responses at various pulse frequencies were analyzed. Figure 5 shows the potential response of pulse frequency at (a) 10, (b) 100, (c) 1000, and (d) 10,000 Hz and depicts the on-time cathodic potential is more negative, indicating larger overpotential, with decreasing pulse frequency. For instance, the cathodic potential of pulse frequency at 10 Hz and 10,000 Hz are around −0.3 and −0.21 V, respectively. It is well-known that the double layer effect is noticeable at high pulse frequency. Therefore, the overpotential is higher at low pulse frequency compared to at high pulse frequency due to maintaining the same output of average current density. Tantavichet et al.[30-32] have also observed that the overpotentail at low pulse frequency was always higher than at high pulse frequency in the plating bath with or without additives. Moreover, additive behavior may be influenced by different overpotentials either in dc or PC conditions. For instance, Moffat et al.[33,34] have reported the influence of potential on the kinetics of accelerator adsorption or activation. Two voltammograms were collected for different switching potentials (E_S), −0.3 V and −0.21 V, based on the results of Fig. 5. The hysteretic current density-voltage behavior for copper deposition in electrolyte containing SPS-PEG-Cl has been described previously.[6,35,36] It is well-known that the distinct hysteretic response, where the deposition rate increases substantially during reverse sweep, arises from displacement of an inhibiting Cl^-—Cu^+—PEG layer by the adsorption of sulfonate-terminated short chain thiol of disulfide molecules.[35-39] As shown in Fig. 6, it is clear that a marked increase in hysteresis is evident for $E_S = -0.3$ V compared with $E_S = -0.21$ V, meaning that the metal deposition rates

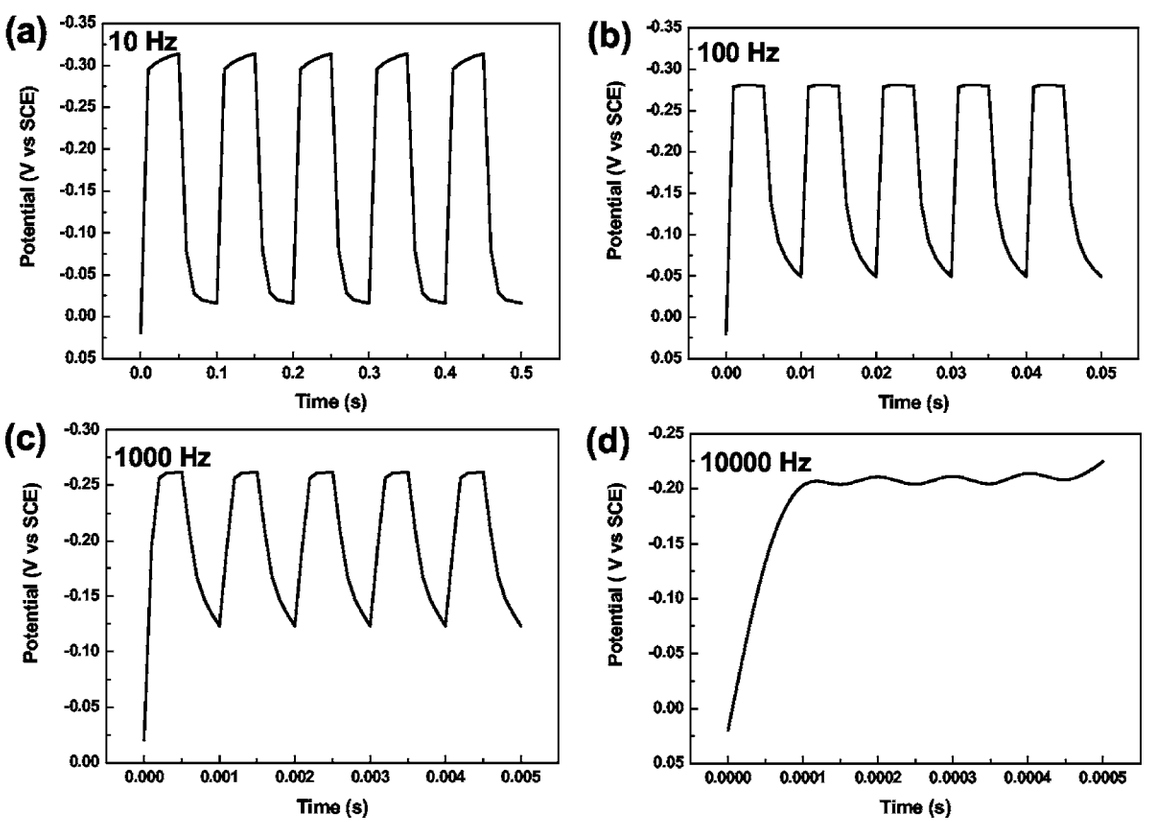

Figure 5. Potential responses with time at various pulse frequencies in the bath with additives, SPS + PEG + Cl^-. The applied average current density is 10 mA/cm^2.

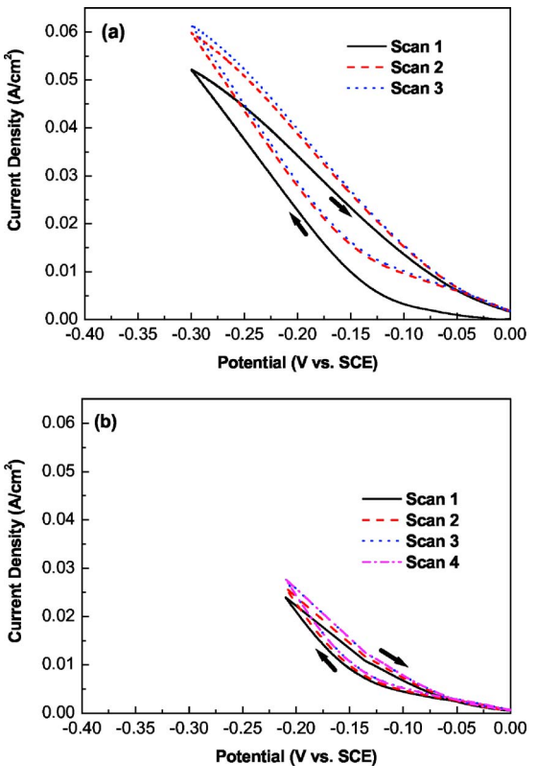

Figure 6. (Color online) Variation of voltammetric switching potential [(a) −0.3 V, (b) −0.21 V] in the SPS-PEG-Cl system. The sweep rate was 1 mV/s.

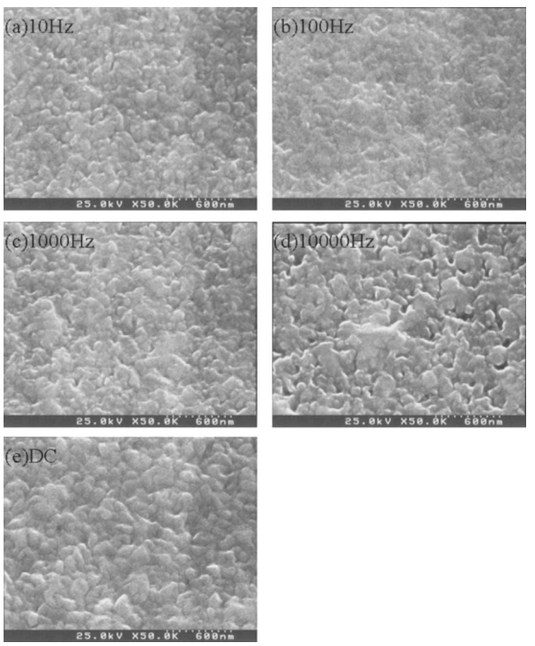

Figure 7. Surface morphology of copper deposit with PC plating at various frequencies as well as with dc at 10 mA/cm^2 in the bath with additives, SPS + PEG + Cl^-.

that characterize the return sweep for $E_S = -0.3$ V is high. This result demonstrates that the kinetics of displacement of the inhibiting Cl^-—Cu^+—PEG layer by SPS adsorption are an increasing function of potential; voltammetric cycling indicates an increase in the SPS surface coverage with higher current on the return sweep. In addition, the hysteresis in Fig. 6 appears to be slightly reduced on the outward sweep; it may be explained by the addition of more Cl^- through leakage from reference electrode.

From the results of Fig. 5, the on-time overpotential increased with decreasing pulse frequency. The results of Fig. 6 indicate that more SPS adsorbed by displacing Cl^-—Cu^+—PEG layer at low pulse frequencies, 10 or 100 Hz, compared with high pulse frequency, 10,000 Hz, or dc due to possessing higher overpotential. Consequently, more desorption of Cl^- and PEG took place in the on-time interval at low pulse frequency. Moreover, the desorbed Cl^- and PEG may have better chance to depart from electrode surface in the off-time interval at low pulse frequency because the interval is relatively long and reaches about 50 ms at 10 Hz. This suggests that re-adsorption of Cl^- and PEG in the off-time interval at low pulse frequency may be less than that at high pulse frequency due to more SPS being adsorbed during the on-time interval.

To examine the above reasoning regarding additive behaviors, SEM was applied to investigate the surface morphology of copper deposit at various pulse frequencies. Figure 7 shows the SEM of copper deposit with PC at (a) 10, (b) 100, (c) 1000, and (d) 10,000 Hz and with (e) dc, where the applied average current density was 10 mA/cm^2. The grains shown in Fig. 7a and b are relatively small and Fig. 7c-e show large grains. Dow et al.[40] reported that fined-grained copper deposit was caused by the accelerator-dominant composition, SPS, and the coarse-grained copper deposit was derived from the suppressor-dominant composition, PEG + JGB + Cl^-. Cabrielli et al.[41] also observed the addition of accelerator resulted in grain refinement, however, the suppressor led to large grain size. This implies that the copper deposit with large grains may result from the suppressor-dominant composition on the surface of copper deposit. The results of Fig. 7 indicate that more Cl^-—Cu^+—PEG complexes were disrupted by SPS at low pulse frequencies, attributing to more Cl^- and PEG desorption. On the other hand, more SPS adsorbed on the surface of deposit, leading to more Cl^- and PEG desorption in the on-time interval at high pulse frequency based on competitive adsorption theory.

The adsorption or desorption behaviors of additives on plated surface can result the incorporation of impurities into the copper deposit. SIMS analysis was performed to further verify the above mechanism. Figure 8 presents the secondary ion counts of additive-derived impurities, sulfur and chloride. At 10 and 100 Hz, the sulfur signals are high. The high sulfur signals mainly arise from the sulfur groups in SPS. In contrast, the chloride signals are low at 10 and 100 Hz. Based on the results of Fig. 8, more SPS displaced PEG on the surface of copper deposit with PC at low pulse frequency. In fact, Gewirth et al.[42] also observed the SPS was included in the film and altered the morphology of deposited film. Therfore, the experimental results of SIMS are consistent with the results of SEM. Furthermore, Moffat et al.[33] have also reported the incorporation of SPS depends on potential. The more negative overpotential resulted in the increase of incorporation of SPS. The results of Fig. 8 are consistent with the report, more incorporation of SPS are presented at low pulse frequency.

Based on the above-mentioned results, copper deposit with high (111)/(200) ratio, which shows high chemical resistance against formation of void defects after CMP can be obtained with use of PC at frequency lower than 100 Hz. However, the use of PC at low frequency may cause adverse effect on filling features since the displacement of PEG by SPS on the surface outside of features would be enhanced with the use of PC at low pulse frequency, thus disrupting the original mechanism of additives, which are utilized to form superconformal deposition. Therefore, the insufficient inhibition on the opening of the features would attribute to the generation of voids or seams in the features. As a result, we proposed a deposition scheme which could minimize the void defects after CMP and still maintain high filling performance. The basic scheme is to utilize

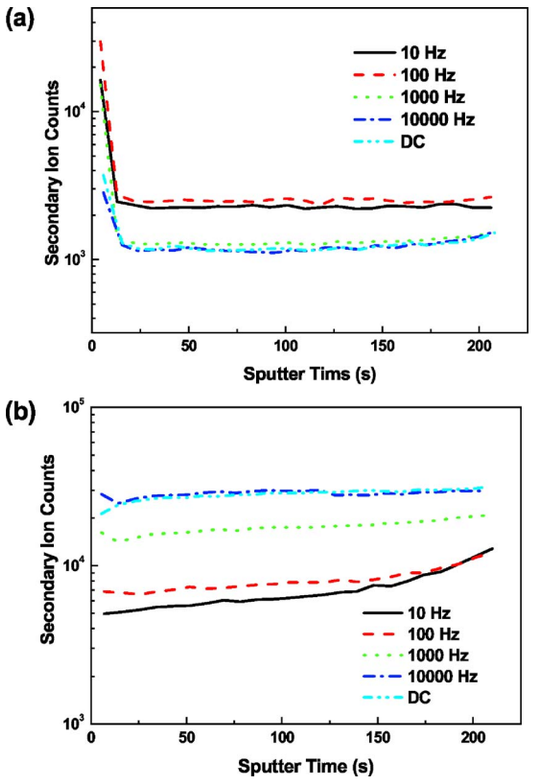

Figure 8. (Color online) Secondary ion counts for (a) sulfur and (b) chloride in copper deposits at various pulse frequencies in the bath with additives, SPS + PEG + Cl^-, are plotted against the sputtering time. The applied average current density is 10 mA/cm^2.

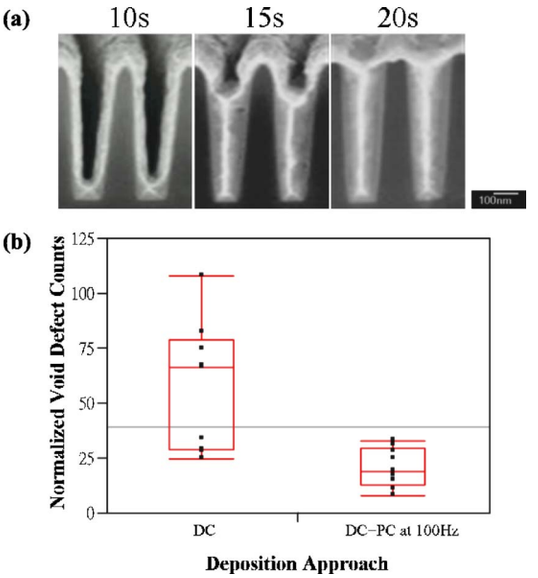

Figure 9. (Color online) (a) SEM images of filling experiments in different deposition time. (b) Box plot comparison between only dc and dc + PC at 100 Hz pulse frequency deposition approach for the formation of void defects on pattern wafers.

dc to fill the features and then use PC at later stage of deposition. Prior to performing the approach, the switched time from dc to PC should be determined. A series of filling experiments with time is shown in Fig. 9a. Initially, the adsorbed SPS was converted to sodium salt (MPS) by external electrons and started its role as a catalyst.[43-46] After ~10 s, the dimerized MPS during the Cu^{2+} reduction adsorbed again at the neighboring site and repeated the cycle. Hence, the dimerized MPS, once adsorbed in the features, did not escape from the features and was accumulated during the progress of deposition. The well-known curvature-enhanced accelerator coverage mechanism was well studied.[4,5,36,47] Consequently, void-free deposition was achieved, as shown in Fig. 9a. Based on Fig. 9a, the recommended switch time is ~20 s. When the switch time was set at 20 s, the dc/PC at 100 Hz was performed and compared with the result with dc only, shown in Fig. 9b. The result indicates that the proposed approach indeed produces fewer void defects after CMP than convectional dc process.

Conclusions

Deposition of highly (111) oriented copper layer is required for achieving better electromigration resistance and lower resistivity. Moreover, the amount of void defects after CMP decreases with the (111)/(200) ratio increasing. We have found while the pulse frequency is lower than 100 Hz, high ratio of (111)/(200) is obtained. However, the use of PC at low pulse frequency would interfere with the void-free deposition in the features because the more displacement of suppressors by accelerators took place at low pulse frequency, which possessed high overpotential. Furthermore, we have proposed a deposition approach to reduce void defects in CMP process based on experimental results. DC is utilized to fill the features in the first step, and then the PC at 100 Hz pulse frequency is applied to accomplish the whole deposition. The performed result of the approach suggests that the reduction of void defects after CMP process could be achieved with the use of the deposition approach.

Acknowledgments

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